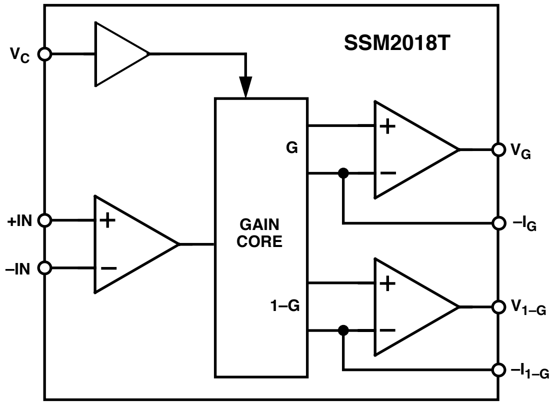
ANALOG
DEVICES

Trimless
Voltage Controlled Amplifiers

SSM2018T*

FEATURES
- **117 dB Dynamic Range**
- **0.006% Typical THD+N (@ 1 kHz, Unity Gain)**
- **140 dB Gain Range**
- **No External Trimming Required**
- **Differential Inputs**
- **Complementary Gain Outputs**
- **Buffered Control Port**
- **I–V Converter On-Chip**
- **Low External Parts Count**
- **Low Cost**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The SSM2018T represents continuing evolution of the Frey Operational Voltage Controlled Element (OVCE) topology that permits flexibility in the design of high performance volume control systems. The SSM2018T is laser trimmed for gain core symmetry and offset. As a result, the SSM2018T is the first professional audio quality VCA to offer trimless operation.

Due to careful gain core layout, the SSM2018T combines the low noise of Class AB topologies with the low distortion of Class A circuits to offer an unprecedented level of sonic transparency. Additional features include differential inputs, a 140 dB (–100 dB to +40 dB) gain range and a high impedance control port. The SSM2018T provides an internal current-to-voltage converter. Thus no external active components are required.

This device is offered in 16-lead plastic DIP and SOIC packages and guaranteed for operation over the extended industrial temperature range of –40°C to +85°C.

NEW E GRADE
0.01% THD+N MAX

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*Protected by U.S. Patent Nos. 4,471,320 and 4,560,947.

REV. B

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SSM2018T–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

(V_S = ±15 V, A_V = 0 dB, R_L = 100 kΩ, f = 1 kHz, 0 dBu = 0.775 V rms, simple VCA application circuit with 18 kΩ resistors, $-V_{IN}$ floating, and Class AB gain core bias (R_B = 150 kΩ), –40°C < T_A < +85°C, unless otherwise noted. Typical specifications apply at T_A = 25°C.)

Parameter	Conditions	Min	Typ	Max	Max (E Grade)	Unit
AUDIO PERFORMANCE						
Noise	V_{IN} = GND, 20 kHz Bandwidth		–95	–93		dBu
Headroom	Clip Point = 1% THD + N		22			dBu
Total Harmonic Distortion plus Noise	2nd and 3rd Harmonics Only (25°C to 85°C)					
	A_V = 0 dB, V_{IN} = +10 dBu		0.006	0.020	0.01	%
	A_V = +20 dB, V_{IN} = –10 dBu		0.013	0.03	0.02	%
	A_V = –20 dB, V_{IN} = +10 dBu		0.013	0.03	0.02	%
INPUT AMPLIFIER						
Bias Current	V_{CM} = 0 V		0.25	1		µA
Offset Voltage	V_{CM} = 0 V		1	15		mV
Offset Current	V_{CM} = 0 V		10	100		nA
Input Impedance			4			MΩ
Common-Mode Range			±13			V
Gain Bandwidth	VCA Configuration		0.7			MHz
	VCP Configuration		14			MHz
Slew Rate			5			V/µs
OUTPUT AMPLIFIER						
Offset Voltage	V_{IN} = 0 V, V_C = 4 V		1.0	15		mV
Output Voltage Swing	I_{OUT} = 1.5 mA					
	Positive	10	13			V
	Negative	–10	–14			V
Minimum Load Resistance	For Full Output Swing		9			kΩ
CONTROL PORT						
Bias Current			0.36	1		µA
Input Impedance			1			MΩ
Gain Constant	Device Powered in Socket > 60 sec		–30			mV/dB
Gain Constant Temperature Coefficient			–3500			ppm/°C
Control Feedthrough	0 dB to –40 dB Gain Range		±1	±4	±3	mV
Maximum Gain	V_C = –1.3 V		40			mV
Maximum Attenuation	V_C = 4 V		100			dB
POWER SUPPLIES						
Supply Voltage Range		±5		±18		V
Supply Current			11	15		mA
Power Supply Rejection Ratio			80			dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	
Dual Supply	±18 V
Input Voltage	$\pm V_S$
Operating Temperature Range	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 60 sec)	300°C

THERMAL CHARACTERISTICS

Thermal Resistance[2]	
16-Lead Plastic DIP	
θ_{JA}	76°C/W
θ_{JC}	33°C/W
16-Lead SOIC	
θ_{JA}	92°C/W
θ_{JC}	27°C/W

TRANSISTOR COUNT

Number of Transistors	
SSM2018T	125

ESD RATINGS

883 (Human Body) Model	500 V
EIAJ Model	100 V

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] θ_{JA} is specified for worst-case conditions, i.e.; θ_{JA} is specified for device in socket for P-DIP and device soldered in circuit board for SOIC package.

ORDERING GUIDE

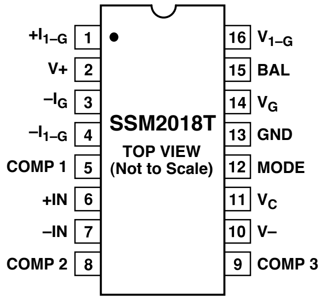
Model	Temperature Range	Package Option[1]
SSM2018TP	–40°C to +85°C	N-16
SSM2018TS[2]	–40°C to +85°C	R-16

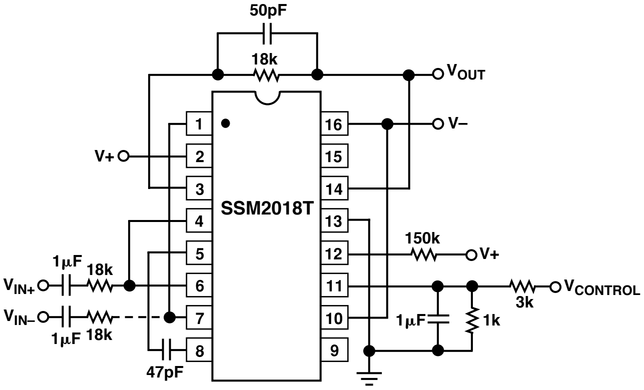
[1] N = Plastic DIP; R = SOL.

[2] Not for new designs; obsolete April 2002.

PIN CONFIGURATION

16-Lead Plastic DIP and SOL



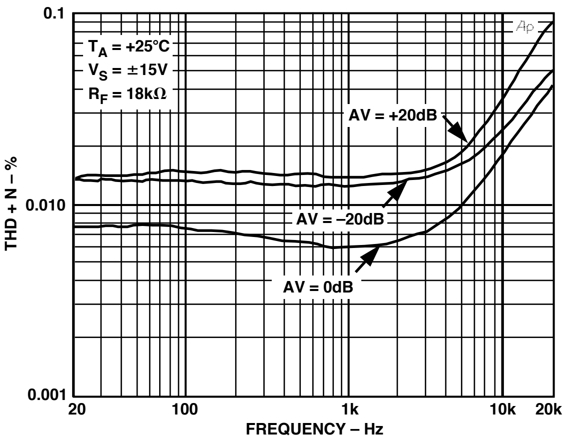


SSM2018T Typical Application Circuit

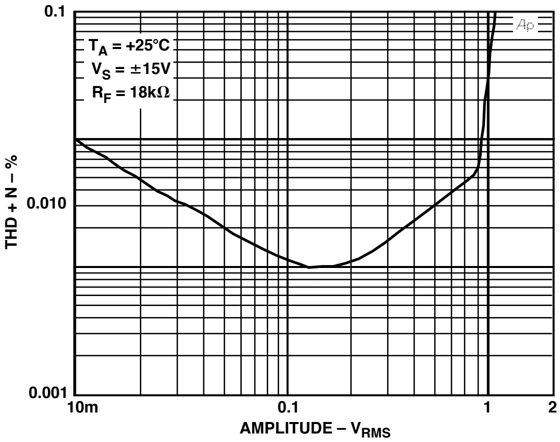
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2018T features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

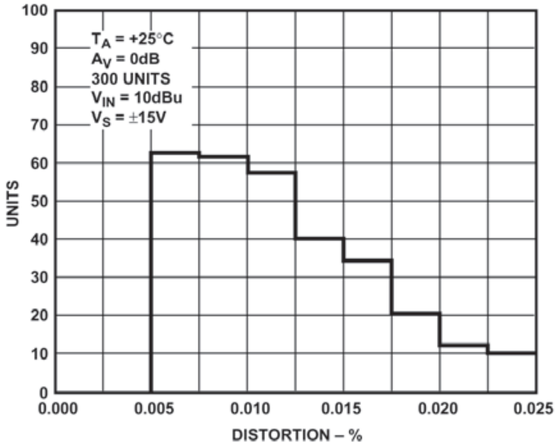
SSM2018T–Typical Performance Characteristics



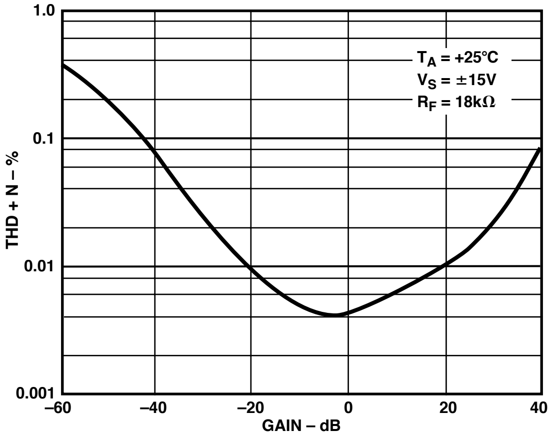
TPC 1. SSM2018T THD + N Frequency (80 kHz Low-Pass Filter, for A_V = 0 dB, V_{IN} = 3 V rms; for A_V = +20 dB, V_{IN} = 0.3 V rms; for A_V = –20 dB, V_{IN} = 3 V rms)



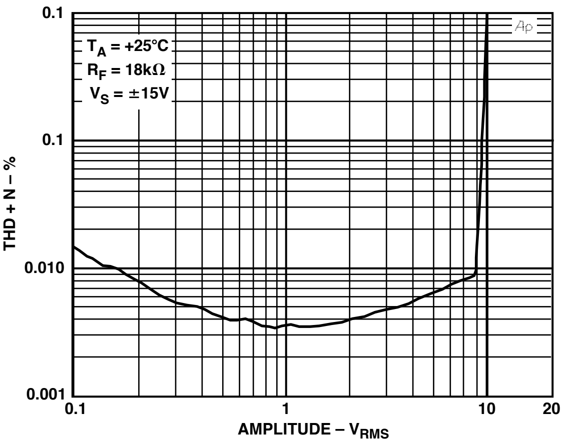
TPC 4. SSM2018T THD + N vs. Amplitude (Gain = +20 dB, f_{IN} =1 kHz, 80 kHz Low-Pass Filter)



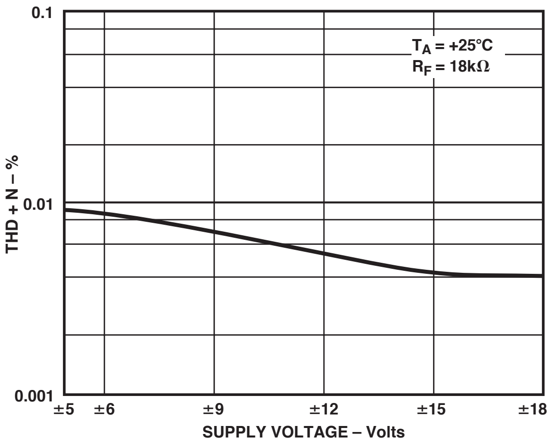
TPC 2. SSM2018T Distortion Distribution



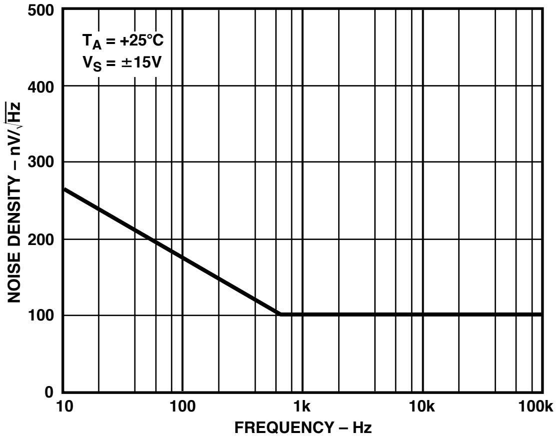
TPC 5. SSM2018T THD + N vs. Gain (f_{IN} = 1 kHz; for –60 dB ≤ A_V ≤ –20 dB, V_{IN} = 10 V rms; for 0 dB ≤ A_V ≤ +20 dB, V_{IN} = 1 V rms)



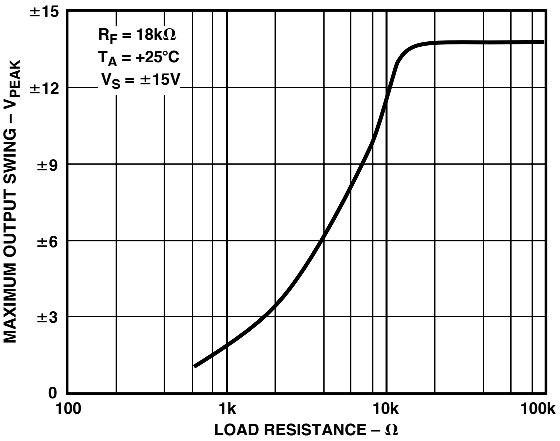
TPC 3. SSM2018T THD + N vs. Amplitude (Gain = 0 dB, f_{IN} = 1 kHz, 80 kHz Low-Pass Filter)



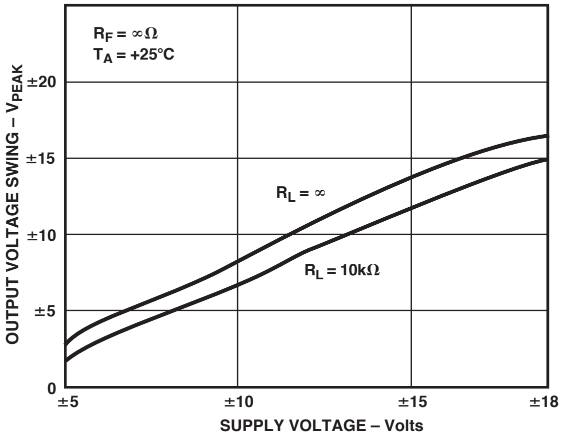
TPC 6. SSM2018T THD + N vs. Supply Voltage (A_V = 0 dB, V_{IN} = 1 V rms, f_{IN} = 1 kHz, 80 kHz Low-Pass Filter)



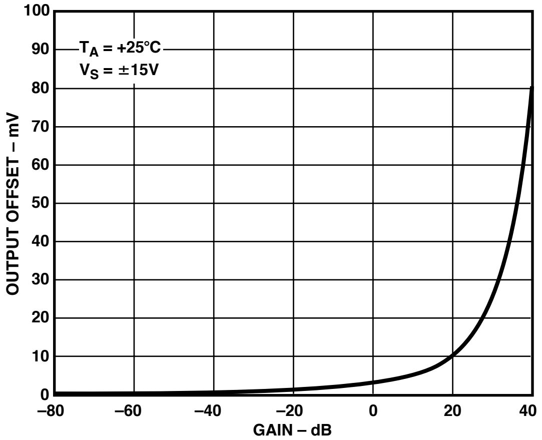
TPC 7. SSM2018T Noise Density vs. Frequency (Unity Gain, Referred to Input)



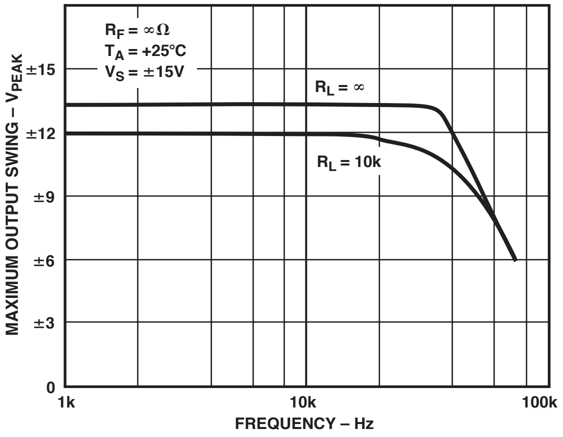
TPC 10. SSM2018T Maximum Output Swing vs. Load Resistance (THD = 1 % max)



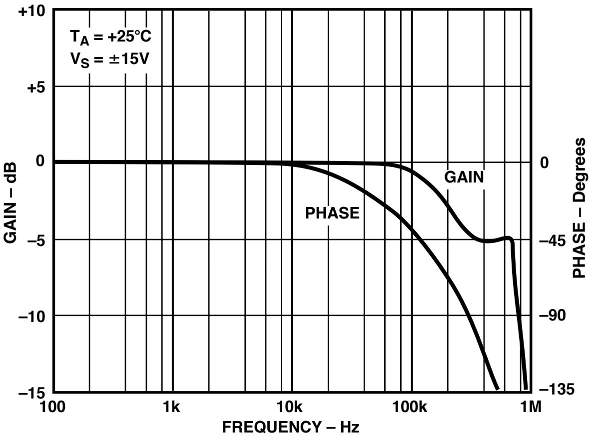
TPC 8. SSM2018T Maximum Output Swing vs. Supply Voltage (THD = 1% max)



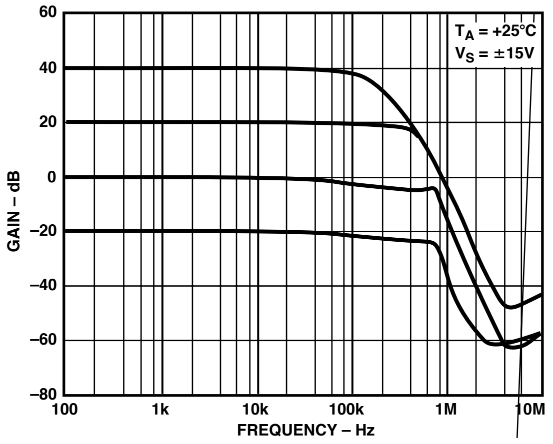
TPC 11. SSM2018T Typical Output Offset vs. Gain



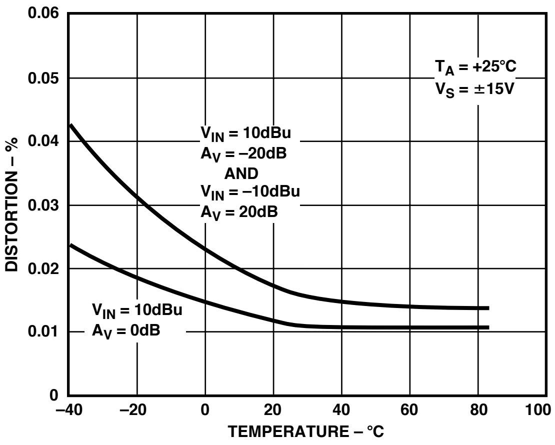
TPC 9. SSM2018T Maximum Output Swing vs. Frequency (THD = 1 % max)



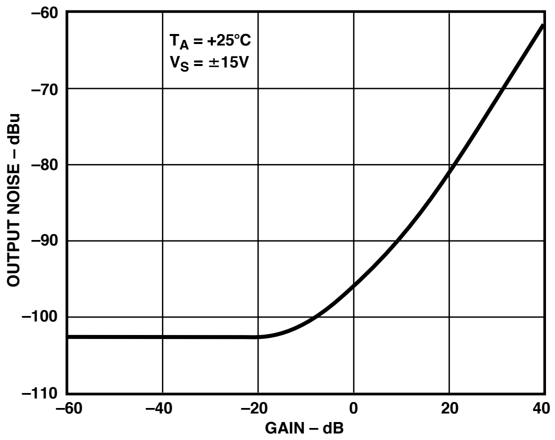
TPC 12. SSM2018T Gain/Phase vs. Frequency



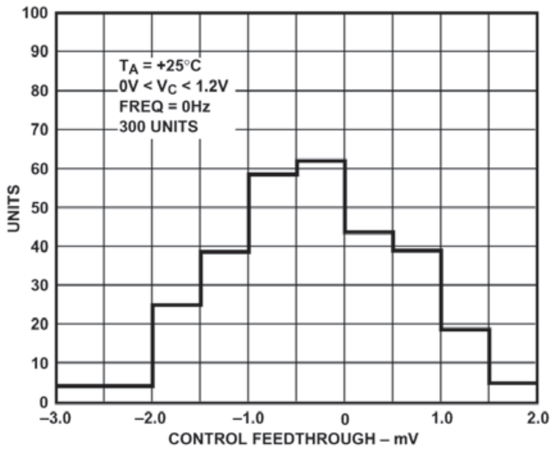
TPC 13. SSM2018T Gain vs. Frequency



TPC14. SSM2018T Distortion vs. Temperature



TPC 15. SSM2018T Output Noise vs. Gain (V_{IN} = GND, 20 kHz Bandwidth)



TPC 16. SSM2018T Control Feedthrough Distribution

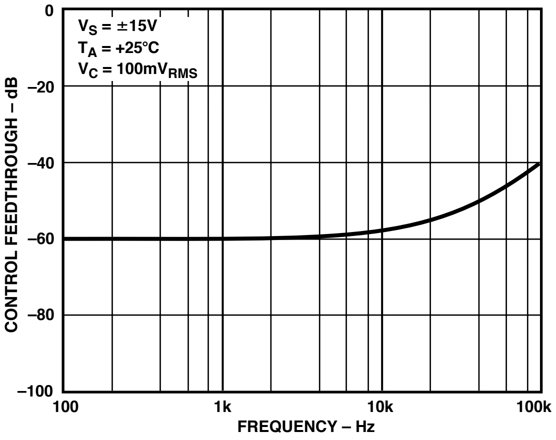
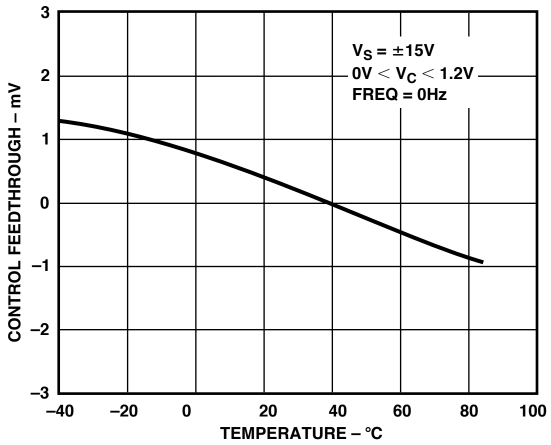
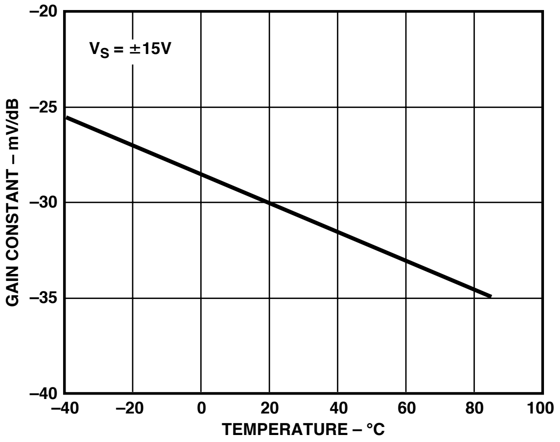


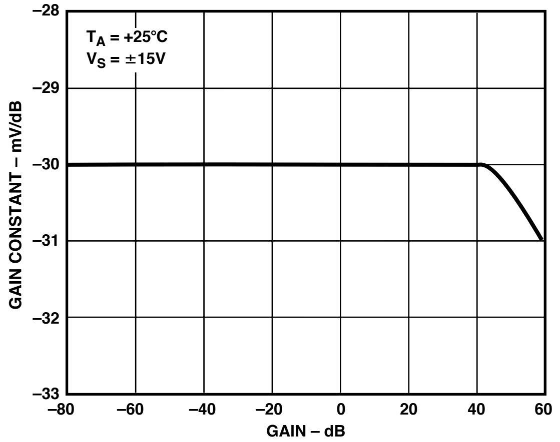
Figure 17. SSM2018T Control Feedthrough vs. Frequency



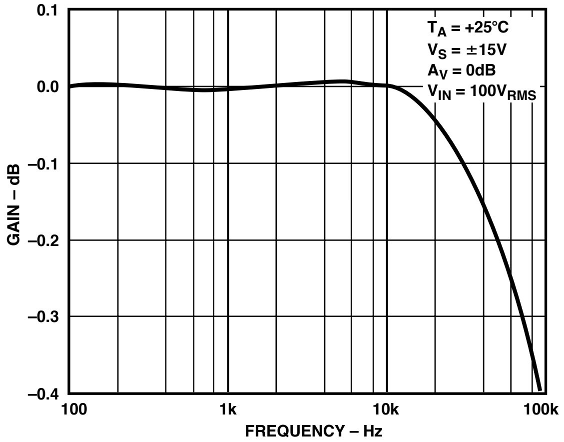
TPC 18. SSM2018T Control Feedthrough vs. Temperature



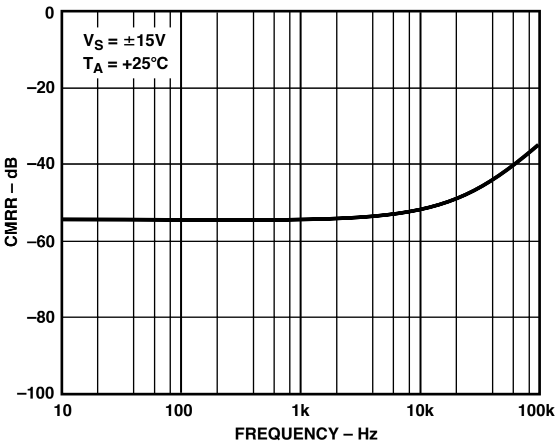
TPC 19. SSM2018T Gain Constant vs. Temperature



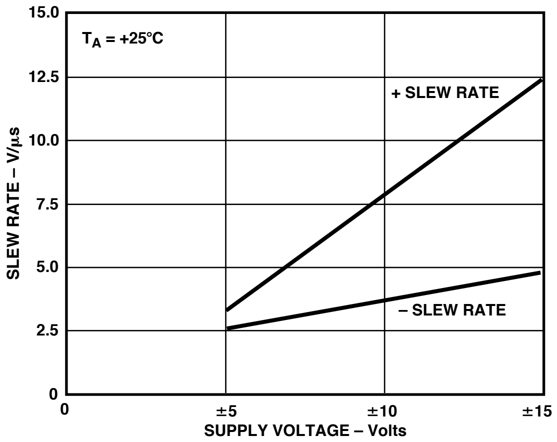
TPC 20. SSM2018T Gain Constant Linearity vs. Gain



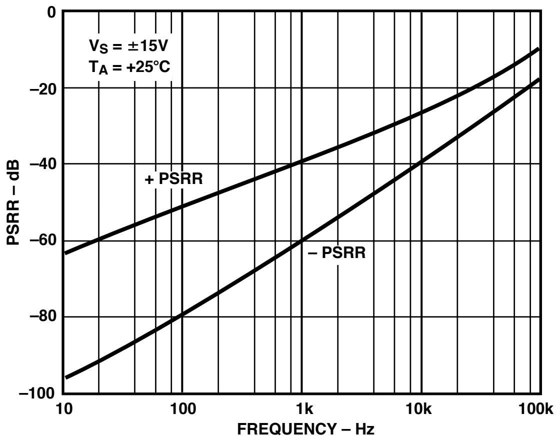
TPC 21. SSM2018T Gain Flatness vs. Frequency



TPC 22. SSM2018T CMRR vs. Frequency



TPC 23. SSM2018T Slew Rate vs. Supply Voltage



TPC 24. SSM2018T PSRR vs. Frequency

APPLICATIONS

The SSM2018T is a *trimless* Voltage Controlled Amplifier (VCA) for volume control in audio systems. The SSM2018T is identical to the original SSM2018 in functionality and pinout; however, it is the first professional quality audio VCA in the marketplace that does not require an external trimming potentiometer to minimize distortion. Instead, the SSM2018T is laser trimmed before it is packaged to ensure the specified THD and control feedthrough performance. This has a significant savings in not only the cost of external trimming potentiometers, but also the manufacturing cost of performing the trimming during production.

Basic VCA Configuration

The primary application circuit for the SSM2018T is the basic VCA configuration, which is shown in Figure 1. This configuration uses differential current feedback to realize the VCA. A complete description of the internal circuitry of the VCA, and this configuration, is given in the Theory of Operation section below. *The SSM2018T is trimmed at the factory for operation in the basic VCA configuration with class AB biasing.* Thus, for optimal distortion and control feedthrough performance, the same configuration and biasing should be used. All of the graphs for the SSM2018T in the data sheet have been measured using the circuit of Figure 1.

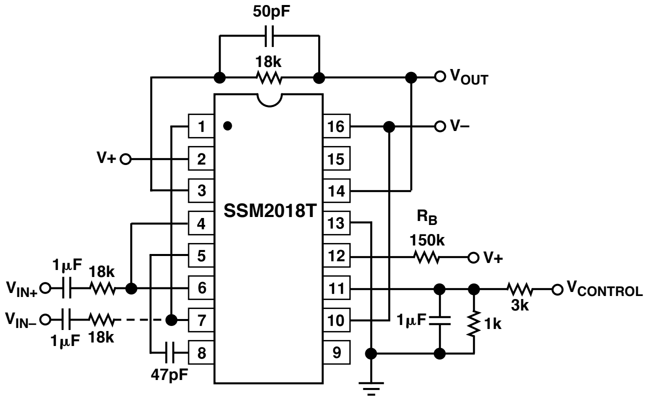


Figure 1. Basic VCA Application Circuit

In the simple VCA configuration, the SSM2018T inputs are at a virtual ground. Thus, 18 kΩ resistors are required to convert the input voltages to input currents. The schematic also shows ac coupling capacitors. These are inserted to minimize dc offsets generated by bias current through the resistors. Without the capacitors, the dc offset due to the input bias current is typically 5 mV. The input stage has the flexibility to run either inverting, noninverting, or balanced. The most common configuration is to run it in the noninverting single-ended mode. If either input is unused, the associated 18 kΩ resistor and coupling capacitor should be removed to prevent any additional noise.

The common-mode rejection in balanced mode is typically 55 dB up to 1 kHz, decreasing at higher frequencies as shown in TPC 21. To ensure good CMRR in the balanced configuration, the input resistors must be balanced. For example, a 1% mismatch results in a CMRR of 40 dB. To achieve 55 dB, these resistors should have an absolute tolerance match of 0.1%.

The output of the basic VCA is taken from Pin 14, which is the output of an internal amplifier. Notice that the second voltage output (Pin 16) is connected to the negative supply. This is normal and actually disables that output amplifier ensuring that it will not oscillate and cause interference problems. Shorting the output to the negative supply does not cause the supply current to increase. This amplifier is only used in the "OVCE" application explained later.

The control port follows a –30 mV/dB control law. The application circuit shows a 3 kΩ and 1 kΩ resistor divider from a control voltage. The choice of these resistors is arbitrary and could be any values to properly scale the control voltage. In fact, these resistors can be omitted if the control voltage has been properly scaled. The 1 µF capacitor is in place to provide some filtering of the control signal. Although the control feedthrough is trimmed at the factory, the feedthrough increases with frequency (TPC 16). Thus, high frequency noise can feed through and add to the noise of the VCA. Filtering the control signal helps minimize this noise source.

Theory of Operation of the SSM2018T

The SSM2018T has the same internal circuitry as the original SSM2018. The detailed diagram in Figure 2 shows the main components of the VCA. The essence of the SSM2018T is the gain core, which comprises two differential pairs (Q1–Q4). When the control voltage, V_C, is adjusted, current through the gain core is steered to one side or the other of the two differential pairs. The tail current for these differential pairs is set by the mode bias of the VCA (Class A or AB), which is labeled as I_M in the diagram. I_M is then modulated by a current proportional to the input voltage, labeled I_S. For a positive input voltage, more current is steered (by the "Splitter") to the left differential pair; the opposite is true for a negative input.

To understand how the gain control works, a simple example is best. Take the case of a positive control voltage on Pin 11. Notice that the bases of Q2 and Q3 are connected to ground via a 200 Ω resistor. A positive control voltage produces a positive voltage on the bases of Q1 and Q4. Concentrating on the left-most differential pair, this raises the base voltage of Q1 above that of Q2. Thus, more of the tail current is steered through Q1 than through Q2. The current from the collector of Q2 flows through the external 18 kΩ feedback resistor around amplifier A3. When this current is reduced, the output voltage is also reduced. Thus, a positive control voltage results in an attenuation of the input signal, which explains why the gain constant is negative.

The collector currents of Q2 and Q3 produce the output voltage. The output of Q3 is mirrored by amplifier A1 to add to the overall output voltage. On the other hand, the collector currents of Q1 and Q4 are used for feedback to the differential inputs. Because Pins 6 and 4 are shorted together, any input voltage produces an input current which flows into Pin 4. The same is true for the inverting input, which is connected to Pin 1. The overall feedback ensures that the current flowing through the input resistors is balanced by the collector currents in Q1 and Q4.

Compensating the SSM2018T

The SSM108 has a network that uses an adaptive compensation scheme that adjusts the optimum compensation level for a given gain. The control voltage not only adjusts the gain core steering, it also adjusts the compensation. The SSM2018T has three compensation pins: COMP1, COMP2, and COMP3. COMP3 is normally left open. Grounding this pin actually defeats the adaptive compensation circuitry, giving the VCA a fixed compensation point. The only time this is desirable is when the VCA has fixed feedback, such as the Voltage Controlled Panner (VCP) circuit

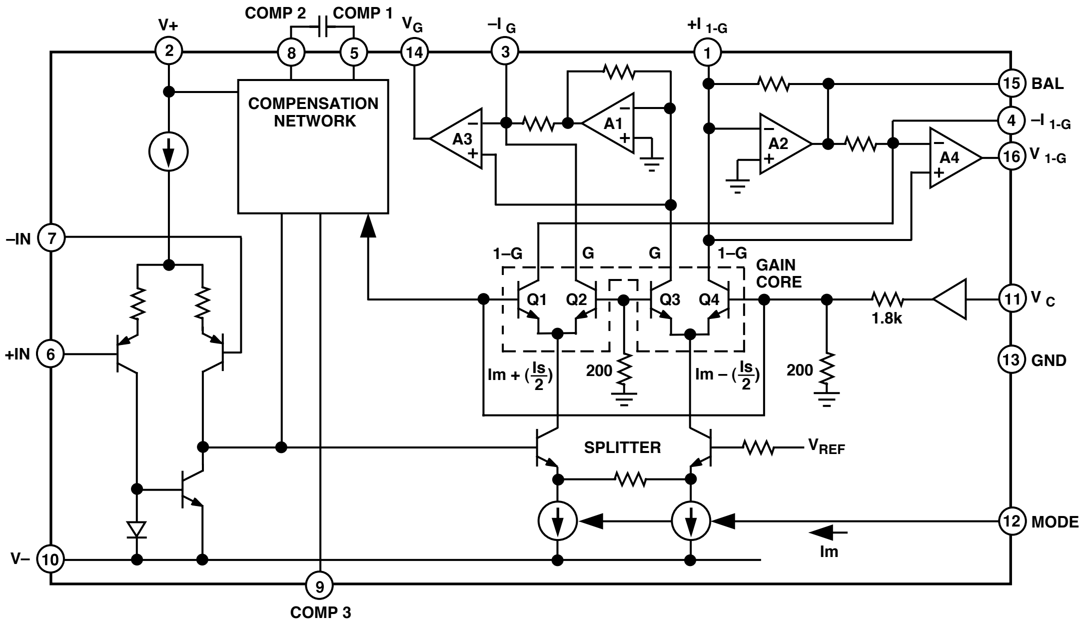


Figure 2. SSM2018T Detailed Functional Diagram

shown later in the data sheet. Thus, for the Basic VCA circuit or the OVCE circuit, COMP3 should be left open.

A compensation capacitor does need to be added between COMP1 and COMP2. Because the VCA operates over such a wide gain range, the compensation should ideally be optimized for each gain. When the VCA is in high attenuation, there is very high "loop gain," and the part needs to have high compensation. On the other hand, at high gain, the same compensation capacitor would overcompensate the part and roll off the high frequency performance. Thus, the SSM2018T employs a patented adaptive compensation circuit. The compensation capacitor is "Miller" connected between the base and collector of an internal transistor. By changing the gain of this transistor via the control voltage, the compensation is changed.

Increasing the compensation capacitor causes the frequency response and slew rate to decrease, which tends to cause high frequency distortion to increase. For the basic VCA circuit, 47 pF was chosen as the optimal value. The OVCE circuit described later uses a 220 pF capacitor. The reason for the increase is to compensate for the extra phase shift from the additional output amplifier used in the OVCE configuration. The compensation capacitor can be adjusted over a practical range from 47 pF to 220 pF if desired. Below 47 pF, the parts may oscillate; above 220 pF the frequency response is significantly degraded.

Control Section

As noted above, the control voltage on Pin 11 steers the current through the gain core transistors to set the gain. The unity gain (0 dB) condition occurs at $V_C = 0$. Attenuation occurs in the VCA for positive voltages (0 V to 3 V, typ), and gain occurs for negative voltage (0 V to –1.3 V, typ). From –1.3 V to +3.0 V, 140 dB of gain range is obtainable. The output gain formula is as follows:

$$V_{OUT} = V_{IN} \times e^{(-aV_C)} \qquad (1)$$

The exponential term arises from the standard Ebers-Moll equation describing the relationship of a transistor's collector current as a function of the base-emitter voltage:

$$I_C = I_S \times e^{(V_{BE}/V_T)} \qquad (2)$$

The factor "*a*" is a function not only of V_T but also the scaling due to the resistor divider of the 200 Ω and 1.8 kΩ resistors shown in Figure 2. The resulting expression for "*a*" is as follows: $a = 1/(10 \times V_T)$, which is approximately equal to 4 at room temperature. Substituting $a = 4$ in the above equation results in a –28.8 mV/dB control law at room temperature.

The –28.8 mV/dB number is slightly different from the data sheet specification of –30 mV/dB. The difference arises from the temperature dependency of the control law. The term V_T is known as the thermal voltage, and it has a direct dependency on temperature: $V_T = kT/q$ (k = Boltzmann's constant = 1.38E–23, q = electron charge = 1.6E–19, and T = absolute temperature in Kelvin). This temperature dependency leads to the –3500 ppm/°C drift of the control law. It also means that the control law changes as the part warms up. Thus, our specification for the control law states that the part has been powered up for 60 seconds.

When the part is initially turned on, the temperature of the die is still at the ambient temperature (25°C for example), but the power dissipation causes the die to warm up. With ±15 V supplies and a supply current of 11 mA, 330 mW is dissipated. This number is multiplied by θ_{JA} to determine the rise in the die's temperature. In this case, the die increases from 25°C to approximately 50°C. A 25°C temperature change causes a 8.25% increase in the gain constant, resulting in a gain constant of 30 mV/dB. The graph in Figure 17 shows how the gain constant varies over the full temperature range.

Proper Operating Mode for the SSM2018T

The SSM2018T has the flexibility of operating in either Class A or Class AB. This is accomplished by adjusting the amount of current flowing in the gain core (I_M in Figure 2). The traditional trade-off between the two classes is that Class A tends to have lower THD but higher noise than Class AB. However, by using well matched gain core transistors, distortion compensation circuitry and laser trimming, the SSM2018T has excellent THD performance in Class AB. Thus, it offers the best of both worlds in having the low noise of Class AB with low THD.

Because the SSM2018T operates optimally in Class AB, the distortion trim is performed for this class. *To guarantee conformance to the data sheet THD specifications, the SSM2018T must be operated in class AB.* This does not mean that it can not be operated in Class A, but the optimal THD trim point is different for the two classes. Using Class A operation results to 0.05% without trim. An external potentiometer could be added to change the trim back to its optimal point as shown in the OVCE application circuit, but this adds the expense and time in adjusting a potentiometer.

The class of operation is set by selecting the proper value for R_B shown in Figure 1. R_B determines the current flowing into the MODE input (Pin 12). For class AB operation with ±15 V supplies, R_B should be 150 kΩ. This results in a current of 95 µA. For other supply voltages, adjust the value of R_B such that current remains at 95 µA. This current follows the formula:

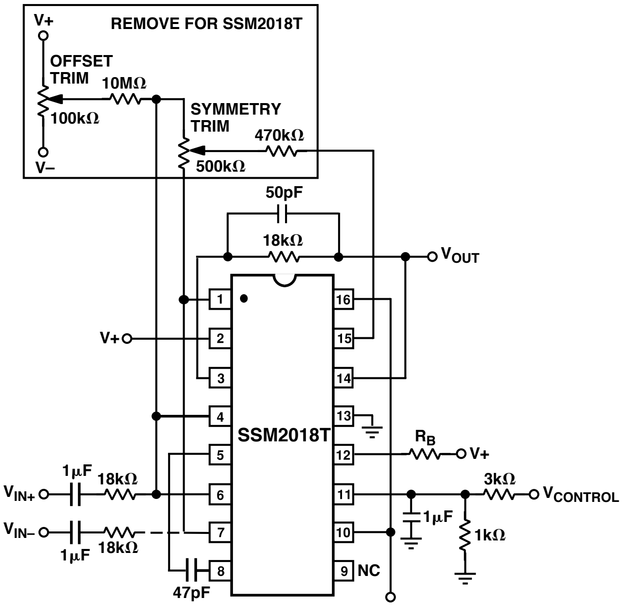
$$I_{MODE} = \frac{(V_{CC} - 0.7\,V)}{R_B} \qquad (3)$$

The factor of 0.7 V arises from the fact that the dc bias on Pin 12 is a diode drop above ground.

Output Drive

The SSM2018T is buffered by an internal op amp to provide a low impedance output. This output is capable of driving to within 1.2 V of either rail at 1% distortion for a 100 kΩ load. Note: This 100 kΩ load is in parallel with the feedback resistor of 18 kΩ, so the effective load is 15.3 kΩ. For better than 0.01% distortion, the output should remain about 3.5 V away from either rail as shown in TPC 2. As the graph of output swing versus load resistance shows (TPC 9), to maintain less than 1% distortion the output current should be limited to approximately ±1.3 mA. If higher current drive is required, the output should be buffered with a high quality op amp such as the OP176 or AD797.

The internal amplifiers are compensated for unity gain stability and are capable of driving a capacitive load up to 4700 pF. Larger capacitive loads should be isolated from the output of the SSM2018T by the use of a 50 Ω series resistor.



R_B: 150kΩ FOR CLASS AB

NC = NO CONNECT

Figure 3. Upgrading SSM2018 Sockets

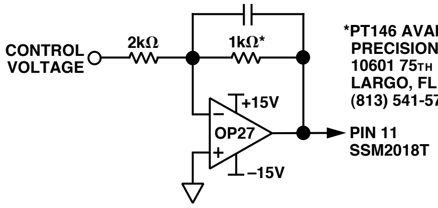
Upgrading SSM2018 Sockets

The SSM2018T easily replaces the SSM2018 in the basic VCA configuration. The parts are pin for pin compatible allowing direct replacement. At the same time, the trimming potentiometers for symmetry and offset should be removed, as shown in Figure 3. Upgrading immediately to the SSM2018T saves the expense of the potentiometers and the time in production of trimming for minimum distortion and control feedthrough.

If the SSM2018 is used in the OVCE or VCP configuration, the SSM2018T can still directly replace it; however, the potentiometers cannot necessarily be removed, as explained in the OVCE and VCP sections.

Temperature Compensation of the Gain Constant

As explained above, the gain constant has a –3500 ppm/°C temperature drift due to the inherent nature of the control port. Over the full temperature range of –40°C to +85°C, the drift causes the gain to change by 7 dB if the part is in a gain of ±20 dB. If the application requires the gain constant to be the same over a wide temperature range, external temperature compensation should be employed. The simplest form of compensation is a temperature compensating resistor (TCR) such as the PT146 from Precision Resistor Co. These elements are different than a standard thermistor in that they are linear over temperature to better match the linear drift of the gain constant.



*PT146 AVAILABLE FROM
PRECISION RESISTOR CO.
10601 75TH ST. NORTH
LARGO, FL 34647
(813) 541-5771

Figure 4. Two TCRs Compensate for Temperature Drift of Gain Constant

As explained above, the gain constant has a –3500 ppm/°C that is due to its reciprocal dependence on absolute temperature. This will cause the gain to vary by 7 dB over the temperature range from –40°C to +85°C when the nominal gain at room temperature is set to 20 dB. Of course, the gain change is quite small if the temperature range of operation is restricted. Nevertheless, the TC of the gain constant is easily compensated by buffering the control voltage to the VCA with a circuit having a 3500 ppm/°C temperature coefficient. Figure 4 shows a simple solution to the problem using an op amp with a PT146 temperature compensating resistor from the Precision Resistor Company. Note that this circuit is inverting, which will change the gain constant to a positive quantity. Any other circuit that provides the necessary positive TC will work.

Digital Control of the Gain

A common method of controlling the gain of a VCA is to use a digital-to-analog converter to set the control voltage. Figure 5 shows a 12-bit DAC, the DAC8512, controlling the SSM2018T. The DAC8512 is a complete 12-bit converter in an 8-pin package. It includes an on-board reference and an output amplifier to produce an output voltage from 0 V to 4.095 V, which is 1 mV/bit. Since the voltage is always positive, this circuit only provides attenuation. The resistor divider on the output of the DAC8512 is set to scale the output voltage so that full scale produces 80 dB of attenuation. The resistor divider can be adjusted to provide other attenuation ranges. If a parallel interface is needed, then the DAC8562 may be used or, for a dual DAC, the AD8582.

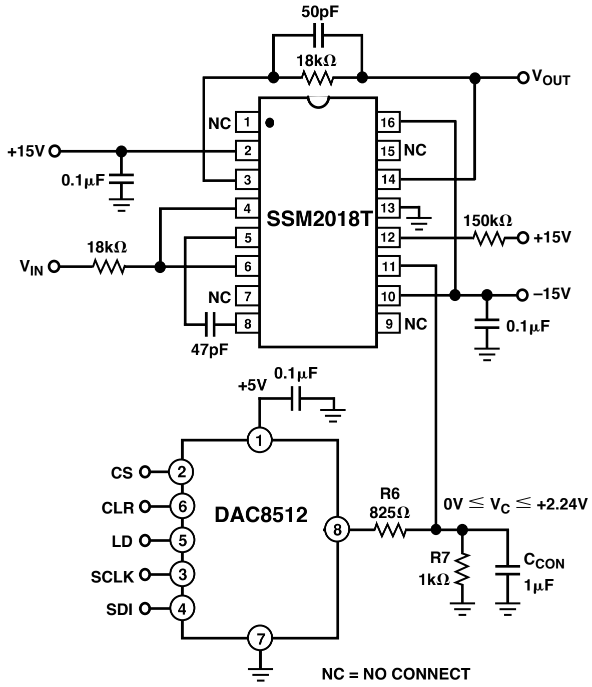


Figure 5. 12-Bit DAC Controls the VCA Gain

Supply Considerations and Single Supply Operation

The SSM2018T has a wide operating supply range. Many of the graphs in this data sheet show the performance of the part from ±5 V to ±18 V. These graphs offer typical performance specifications and are a good indication of the parts' capabilities. The minimum operating supply voltage is ±4.5 V. Below this voltage, the parts are inoperable. Thus, to account for supply variations, the recommended minimum supply is ±5 V.

For simplicity the circuits in the data sheet do not show supply decoupling; however, to ensure best performance, each supply pin should be decoupled with a 0.1 µF ceramic (or other low resistance and inductance type) capacitor as close to the package as possible. This minimizes the chance of supply noise feeding through the part causing excessive noise in the audio frequency range.

The SSM2018T can be operated in single supply mode as long as the circuit is properly biased. Figure 6 shows the proper configuration, which includes an amplifier to create a false ground node midway between the supplies. A high quality, wide bandwidth audio amplifier, such as the OP176 or AD797, should be used to ensure a very low impedance ground over the full audio frequency range. The minimum operating supply for the SSM2018T is ±5 V, which gives a minimum single supply of +10 V and ground. The performance of the circuit with +10 V is identical to graphs that show operation of the SSM2018T with ±5 V supplies.

Operational Voltage Controlled Element

The SSM2018T has considerable flexibility beyond the basic VCA circuit utilized throughout this data sheet. The name "Operational Voltage Controlled Element" comes from the fact that the part behaves much like an operational amplifier with a second voltage controlled output. The symbol for the OVCE connected as a unity gain follower/VCA is shown in Figure 7. The voltage output labeled V_{1-G} is fed back to the inverting input just as it is for an op amp's feedback. The V_G output is amplified or attenuated depending upon the control voltage.

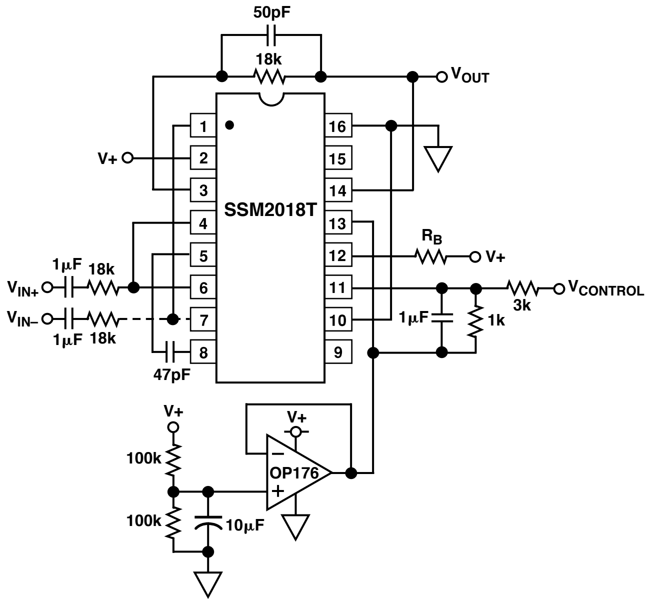


Figure 6. Single Supply Operation of SSM2018T

Because the OVCE works just like an op amp, the feedback could as easily have included resistors to add gain, or a filter network to add frequency shaping. The full circuit for the OVCE is shown in Figure 8. Notice that the amplifier whose output (Pin 16) was originally connected to V_{MINUS} is now the output for feedback. As mentioned before, because the SSM2018T is trimmed for the basic VCA configuration, potentiometers are needed for the OVCE configuration to ensure the best THD and control feedthrough performance.

If a symmetry trim is to be performed, it should precede the control feedthrough trim and be done as follows:

1. Apply a 1 kHz sine wave of 10 dBu to the input with the control voltage set for unity gain.
2. Adjust the symmetry trim potentiometer to minimize distortion of the output signal.

Next the control feedthrough trim is done as follows:

1. Ground the input signal port and apply a 60 Hz sine wave to the control port. The sine wave should have its high and low peaks correspond to the highest gain to be used in the application and 30 dB of attenuation, respectively. For example, a range of 20 dB gain to 30 dB attenuation requires that the sine wave amplitude ranges between –560 mV and +840 mV on Pin 11.
2. Adjust the control feedthrough potentiometer to null the signal seen at the output.

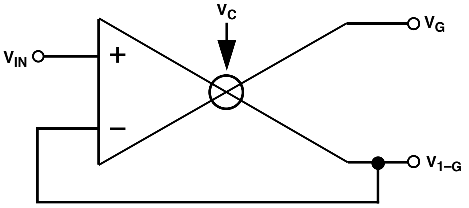


Figure 7. OVCE Follower/VCA Connection

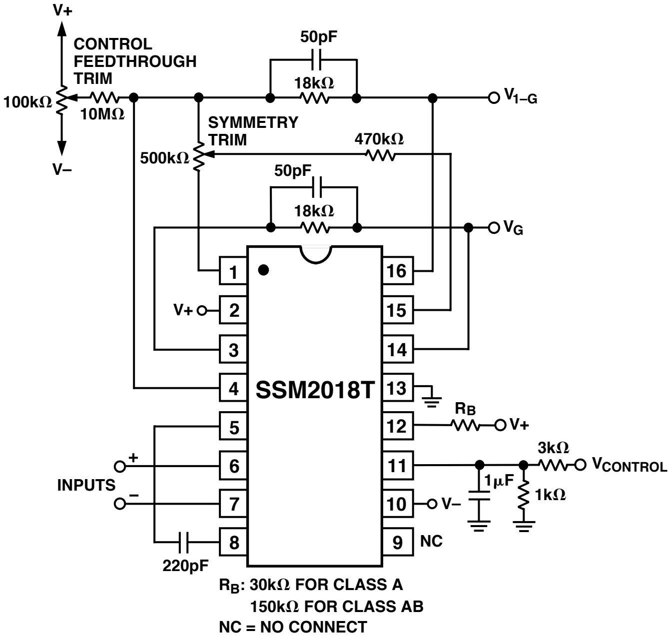


Figure 8. OVCE Application Circuit

Voltage Controlled Panner

An interesting circuit that is built with the OVCE building block is a voltage controlled panner. Figure 9 shows the feedback connection for the circuit. Notice that the average of both outputs is fed back to the input. Thus, the average must be equal to the input voltage. When the control voltage is set for gain at V_G, this causes $V_{1–G}$ to attenuate (to keep the average the same). On the other hand, when V_G is attenuated, $V_{1–G}$ is amplified. The result is that the control voltage causes the input to "pan" from one output to the other. The following expressions show how this circuit works mathematically:

$$V_G = 2\,K \times V_{IN} \text{ and } V_{I-G} = 2\,(1-K) \times V_{IN} \qquad (4)$$

where K varies between 0 and 1 as the control voltage is changed from full attenuation to full gain, respectively. When $V_C = 0$, then $K = 0.5$ and $V_G = V_{1–G} = V_{IN}$. Again, trimming is required for best performance. Pin 9 must be grounded. This is possible because the feedback is constant and the adaptive network is not needed. The VCP is the only application shown in this data sheet where Pin 9 is grounded.

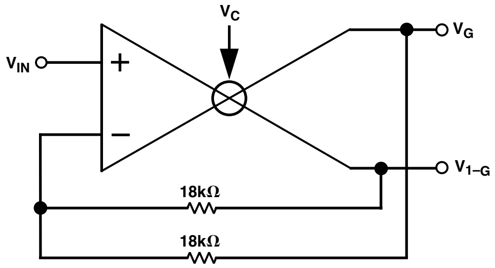
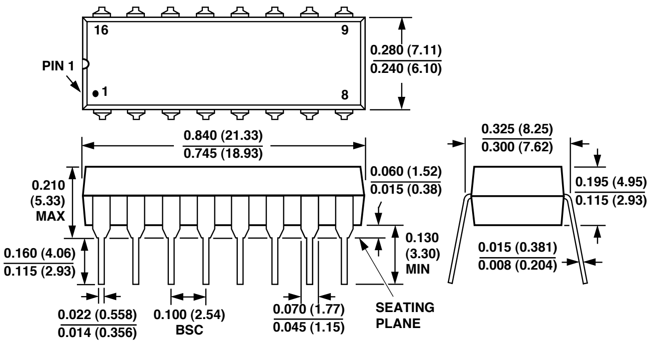


Figure 9. Basic VCP Connection

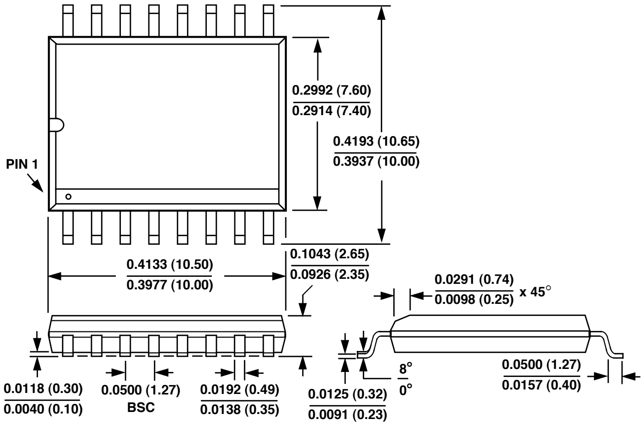
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Plastic DIP (N-16) Package



16-Lead SOIC (R-16) Package



Revision History

Location	Page
7/02—Data Sheet changed from REV. A to REV. B.	
Deleted references to SSM2118T	Global
Edits to FEATURES	1
Edits to GENERAL DESCRIPTION	1
Deleted SSM2118T FUNCTIONAL BLOCK DIAGRAM	1
Deleted 16-Lewad Plastic DIP and SOL from PIN CONFIGURATIONS	3
Edits to ORDERING GUIDE	3
Deleted SSM2118T Typical Application Circuit	3
Deleted TPCs	7–8
Edits to APPLICATIONS	10
Deleted section BASIC VCA CONFIGURATION FOR THE SSM21218T	11

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